Patent claims:

1. A logic basic cell for forming an output signal from at least three input signals in accordance with a predeterminable logic function,

- having a first logic function block having two data signal inputs, to which a first input signal and a second input signal can be applied, and having a data signal output for providing a logic combination of the first input signal and the second input signal in accordance with a predeterminable first logic subfunction;
- having a second logic function block having two data signal inputs, to which the first input signal and the second input signal can be applied, and having a data signal output for providing a logic combination of the first input signal and the second input signal in accordance with a predeterminable second logic subfunction;
- having a first logic transistor having a first source/drain terminal, which is coupled to the data signal output of the first logic function block, having a gate terminal, at which a third input signal can be provided, and having a second source/drain terminal, at which the output signal can be provided;
- having a second logic transistor having a first source/drain terminal, which is coupled to the data signal output of the second logic function block, having a gate terminal, at which a complementary signal with respect to the third input signal can be provided, and having a second source/drain terminal, which is coupled to the second source/drain terminal of the first logic transistor.

2. The logic basic cell as claimed in claim 1, in which the first logic function block and the second logic function block in each case have at least one additional data signal input, it being possible for an additional input signal to be applied to each of the additional data signal inputs, whereby the logic basic cell is set up for forming an output signal from at least four input signals in accordance with a predeterminable logic function.

3. The logic basic cell as claimed in claim 1 or 2, in which the first logic function block and the second logic function block are in each case formed from a plurality of data signal transistors that are connected up to one another in accordance with the respective logic subfunction.

4. The logic basic cell as claimed in claim 3, in which

- the logic transistors and the data signal transistors are transistors of a first conduction type, and the transistors of the first conduction type forming a first data signal path;
- a second data signal path is formed from transistors of a second conduction type, which is complementary to the first conduction type, in which case, for each of the transistors of the first data signal path, a correspondingly connected up transistor is provided in the second data signal path;
- the second source/drain terminals of the logic transistors of the first data signal path and the second source/drain terminals of the logic transistors of the second data signal path are coupled to one another.

5. The logic basic cell as claimed in one of claims 1 to 4, having an evaluation switch, to which the output signal can be applied, and having a precharge switch, which switches are

connected up and can be controlled in such a way that the output signal is provided at an output of the logic basic cell when the evaluation switch is open and the precharge switch is closed, and that a reference signal is provided at the output of the logic basic cell when the precharge switch is open and the evaluation switch is closed.

6. The logic basic cell as claimed in claim 5, in which the evaluation switch and the precharge switch are in each case transistors.

7. The logic basic cell as claimed in one of claims 1 to 6, set up as a CMOS logic basic cell.

8. The logic basic cell as claimed in one of claims 1 to 7, in which at least one of the logic function blocks is formed as

- programmable logic device;
- field-programmable gate array;
- mask-programmed application specific integrated circuit;
- logic gate or arrangement of a plurality of logic gates; or
- look-up table.

9. The logic basic cell as claimed in at least one of claims 1 to 8, in which at least one of the logic function blocks has at least one logic function configuration input by means of which the logic subfunction that can be realized is predetermined in an invariable manner for the respective logic function block.

10. The logic basic cell as claimed in claim 9, having a memory device which is coupled to the at least one

logic function configuration input and in which the information for predetermining the logic subfunction that can be realized can be stored.

11. The logic basic cell as claimed in one of claims 1 to 8, in which at least one of the logic function blocks has at least one logic function configuration input by means of which the logic subfunction that can be realized is predetermined in a variable manner for the respective logic function block by means of a signal that can be applied.

12. The logic basic cell as claimed in one of claims 1 to 11, in which at least one of the logic function blocks furthermore has:

- a first complementary data signal input, to which the logically complementary signal with respect to the first input signal can be applied;
- a second complementary data signal input, to which the logically complementary signal with respect to the second input signal can be applied;
- a first logic selection element between the first data signal input and the second data signal input;
- a second logic selection element between the first data signal input and the second complementary data signal input;
- a third logic selection element between the second data signal input and the first complementary data signal input;
- a fourth logic selection element between the first complementary data signal input and the second complementary data signal input;

it being possible to provide, at the data signal output, the logic combination of the two data signals in accordance with the logic function selected by means of the logic selection

elements.

13. The logic basic cell as claimed in claim 12, in which the logic selection elements are invariable hardware elements.

14. The logic basic cell as claimed in claim 12 or 13, in which the logic selection elements are realized by means of a plurality of metallization planes and/or by means of vias.

15. The logic basic cell as claimed in claim 14, in which

- the first logic selection element is a first logic transistor, which can be controlled by means of a first logic selection signal;
- the second logic selection element is a second logic transistor, which can be controlled by means of a second logic selection signal;
- the third logic selection element is a third logic transistor, which can be controlled by means of a third logic selection signal;
- the fourth logic selection element is a fourth logic transistor, which can be controlled by means of a fourth logic selection signal.

16. The logic basic cell as claimed in one of claims 12 to 15, having four data signal transistors, at the gate terminals of which in each case one of the data signals or one of the logically complementary data signals with respect to one of the data signals can be provided.

17. The logic basic cell as claimed in claim 16,

in which a first data signal transistor is connected up in such a way that its

- first source/drain terminal is coupled to a first source/drain terminal of the first logic transistor and to a first source/drain terminal of the second logic transistor;
- second source/drain terminal is coupled to a first source/drain terminal of a third data signal transistor.

18. The logic basic cell as claimed in claim 17, in which the third data signal transistor is connected up in such a way that its second source/drain terminal is coupled to a first source/drain terminal of the fourth logic transistor and to a first source/drain terminal of the third logic transistor.

19. The logic basic cell as claimed in one of claims 16 to 18, in which a second data signal transistor is connected up in such a way that its

- first source/drain terminal is coupled to a second source/drain terminal of the first logic transistor and to a second source/drain terminal of the third logic transistor;
- second source/drain terminal is coupled to a first source/drain terminal of a fourth data signal transistor.

20. The logic basic cell as claimed in claim 19, in which the fourth data signal transistor is connected up in such a way that its second source/drain terminal is coupled to a second source/drain terminal of the second logic transistor and to a second source/drain terminal of the fourth logic transistor.

21. A logic basic cell array for forming an arrangement output signal from at least four input signals in accordance with a predeterminable logic function,

- having a first logic basic cell as claimed in one of claims 1 to 20;
- having a third logic transistor having a first source/drain terminal, to which the output signal of the first logic basic cell can be applied, having a gate terminal, at which a fourth input signal can be provided, and having a second source/drain terminal, at which the output signal of the logic basic cell array can be provided;
- having a second logic basic cell as claimed in one of claims 1 to 20;
- having a fourth logic transistor having a first source/drain terminal, to which the output signal of the second logic basic cell can be applied, having a gate terminal, at which a complementary signal with respect to the fourth input signal can be provided, and having a second source/drain terminal, which is coupled to the second source/drain terminal of the third logic transistor.

22. A logic device for forming a logic combination of more than four data signals,
having a plurality of logic basic cell arrays as claimed in claim 21.